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Alexander J. Burke			EXAMINER	
Intellectual Property Department			PADMANABHAN, KAVITA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/767,031	Applicant(s) CRESSMAN, RICHARD
	Examiner Kavita Padmanabhan	Art Unit 2161

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 26 March 2008.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 29 January 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-166/08)
 Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Status of Claims

1. Claims 1-20 are pending.
2. Claims 1, 6, 12, and 18 have been amended.
3. Claims 1-20 are rejected.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/26/08 has been entered.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
6. **Claims 1-20** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be support in the applicant's original specification for the limitation, "automatically continuing said sequential storage of data in a second physical storage dataset of said logical dataset *starting at an address automatically determined in response to predetermined instruction and independent of said end storage address*," as recited in independent **claims 1, 6, 12, and 18**. Applicant has pointed to paragraphs [0035], [0061], and [0078]-[0080] of applicant's original specification and to Figure 3, reference character 3400 as containing support for this limitation. Specifically, applicant has stated that par [0078] contains the needed support. The examiner does not find support for this limitation in any of those sections or in any other portions of the applicant's original disclosure. In fact, it appears to the examiner that paragraph [0074] comes closest to discussing the feature claimed. Par [0074] states, in part, "*After reaching the location identified by an end storage address 1440 of physical storage dataset 1400 dataset processor 1200 sequentially stores data in the next subsequent physical storage dataset 1500, 1800 of logical dataset 1300 and 1600 respectively starting at an address subsequent to the end storage addresses 1440, 1740.*" This does not appear to support the claimed limitation and rather seems to contradict the address being independent of the end storage address. Furthermore, the term "predetermined instruction" does not appear throughout the applicant's specification. The dependent claims are rejected in view of their dependence on claims 1, 6, 12, and 18.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Art Unit: 2161

8. **Claims 1-20** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to **claims 1, 6, 12, and 18**, the limitation “automatically *continuing said sequential storage of data* in a second physical storage dataset of said logical dataset starting *at an address* automatically determined in response to predetermined instruction and *independent of said end storage address*” renders the claim unclear. Specifically, it is unclear to the examiner how sequential storage of data is continued in a second physical storage dataset at an address independent of the end storage address of the first physical storage dataset. It would seem to the examiner that for the data to be *sequentially* stored, the starting address of the second physical storage dataset would be subsequent to the end storage address of the first physical storage dataset, and not *independent* of it. The dependent claims are rejected in view of their dependence on claims 1, 6, 12, and 18.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. **Claims 1-8, 12-14, and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over L'Heureux (US 2003/0101193).

In regards to **claim 6**, L'Heureux teaches a method for processing application program data for storage and retrieval employed by a processing device, comprising the steps of:

- designating a logical dataset encompassing a plurality of physical storage datasets (L'Heureux; par [0026], lines 21-23 - *"Large datasets are stored on one or more of the disks 130, 140, or 150"*), each of said plurality of physical storage datasets having a predetermined storage capacity (L'Heureux; par [0027], lines 7-9 – *"each of the disks has 2,000 cylinders which can be allocated for storing a database or dataset"*);
- sequentially storing data in said logical dataset (L'Heureux; par [0027], lines 11-12 – *"the allocation begins with disk 130 and then proceeds to disk 140"*);
- monitoring said sequential storage of data in said logical dataset to determine an occurrence of data storage at a location identified by an end storage address of said first physical storage dataset (L'Heureux; par [0027], lines 11-16 – *"disk 130 will be 100% filled with data from the dataset ... disk 140 will correctly show it is 50% full"* – if starts with disk 1 and fills it up and then proceeds to disk 2, then clearly monitoring when disk 1 has reached its capacity); and
- automatically continuing said sequential storage of data in a second physical storage dataset of said logical dataset starting at an address automatically determined in response to predetermined instruction and independent of said end storage address (L'Heureux; par [0027], lines 11-16 - *"the allocation begins with disk 130 and then proceeds to disk 140 ... disk 140 will correctly show it is 50% full"*; par [0028] – *"For this dataset, it is assumed that allocation begins with disk 150 and then proceeds to disks 130 and 140 in turn. The end result is that disks 130 and 150 are 100% full and disk 140 is 50% full."*

– in this case, the data storage is continued at an address independent of the end storage address of the first physical storage dataset since it goes from disk 150 to a point in disk 130 where the disk is half full, i.e. the address is not related to, or right next to or right after, the end storage address of the first physical storage dataset).

L'Heureux does not expressly teach maintaining an identifier identifying an end storage address of a first physical storage dataset of said logical dataset indicating end of said predetermined storage capacity of said first physical storage dataset.

However, since L'Heureux teaches storing a database or dataset over multiple disks with predetermined storage capacities, it would have been obvious to one or ordinary skill in the art at the time of the applicant's invention to implement the method of L'Heureux by maintaining identifiers to end storage addresses in order to monitor when a disk is full and a new disk must be used.

In regards to **claim 7**, L'Heureux teaches the method according to claim 6, wherein said step of monitoring said sequential storage of data in said logical dataset includes the step of maintaining an identifier of storage capacity used in response to storage of data in said logical dataset (**L'Heureux; par [0026], lines 25-26 – “determining when the combined storage limits of the disks are approached”; par [0070]**).

In regards to **claim 8**, L'Heureux teaches the method according to claim 7, wherein said determination of said occurrence of data storage at said location identified by said end storage address of said first physical storage dataset is performed using said identifier of storage capacity

used and said predetermined storage capacity of said first physical storage dataset (**L'Heureux**; par [0027]; par [0070]).

Claims 1-5 are rejected using the same rationale given for claim 6.

Claims 12-14 are rejected using the same rationale given for claims 6-8, respectively.

Claim 18 is rejected using the same rationale given for claim 6.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. **Claims 9-11, 15-17, 19, and 20** are rejected under 35 U.S.C. 103(a) as being

unpatentable over **L'Heureux** in view of **Plow** (US 4,408,273).

In regards to **claim 9**, **L'Heureux** teaches the method according to claim 6.

L'Heureux does not expressly teach the end storage address comprising a relative address.

Plow teaches using relative byte addresses (RBAs) to address a particular storage location (**Plow; col. 1, lines 32-36**).

It would have been obvious to one or ordinary skill in the art at the time of the applicant's invention to implement the method of **L'Heureux** using relative addresses as a way to address storage locations.

In regards to **claim 10**, L'Heureux teaches the method according to claim 6.

L'Heureux does not expressly teach at least one physical storage dataset comprising an IBM virtual storage access method entry sequenced dataset (VSAM ESDS).

Plow teaches using VSAM ESDS for data set storage (**Plow; col. 2, line 66 – col. 3, line 4; col. 5, lines 11-29**).

It would therefore have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the method of L'Heureux using at least one VSAM ESDS to access the stored data (**Plow; col. 2, line 56 – col. 3, line 4**).

In regards to **claim 11**, L'Heureux teaches the method according to claim 6.

L'Heureux does not expressly teach said identifier identifying an end storage address comprising a pointer.

Plow teaches using pointers to identify a particular storage location (**Plow; col. 1, lines 32-36**).

It would have been obvious to one or ordinary skill in the art at the time of the applicant's invention to implement the method of L'Heureux using pointers as a way to identify storage locations.

Claims 15 and 20 are each rejected using the same rationale given for claim 9.

Claims 16 and 19 are each rejected using the same rationale given for claim 10.

Claim 17 is rejected using the same rationale given for claim 11.

Response to Arguments

13. Applicant's arguments filed 3/26/08 with respect to the prior art rejections of the claims have been fully considered but they are not persuasive.

Applicant argues at page 7 of applicant's remarks that in contrast to the teachings of L'Heureux, the claimed invention does not merely monitor when a dataset is approaching capacity, it automatically switches writing data from one physical dataset onto another. The examiner respectfully disagrees with the applicant's argument and asserts that L'Heureux teaches switching writing data from one physical dataset onto another when the first physical dataset reaches capacity (L'Heureux; par [0027]; par [0028]), thereby meeting the language of the claim as written.

Applicant also argues that the claimed logical dataset incorporates a plurality of physical datasets which may be non-contiguous, e.g. on totally separate disk drives. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *non-contiguous* physical datasets) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, the examiner asserts that L'Heureux does indeed teach that the physical datasets may be separate disk drives (L'Heureux; par [0026], lines 21-23 - "*Large datasets are stored on one or more of the disks 130, 140, or 150*".).

Applicant further argues that the claimed datasets can be processed either randomly or sequentially, whereas the datasets of L'Heureux can only be processed sequentially. The examiner respectfully disagrees with the applicant's argument and asserts that the claims only recite sequential storage of datasets and do not recite "randomly" storing or processing the datasets. Again, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. Therefore, the claims recite sequential storage and L'Heureux teaches sequential storage, meaning that teachings of L'Heureux meet the language of the claims.

Applicant argues at page 8 of applicant's remarks that L'Heureux with Plow does not teach the end storage address comprising a relative address, but has not provided any reasons as to why this specific limitation is allegedly not taught by the cited references. In response, the examiner respectfully disagrees with the applicant's argument and asserts that Plow teaches using relative byte addresses (RBAs) to address a particular storage location (Plow; col. 1, lines 32-36), rendering it obvious to implement the method of L'Heureux using relative addresses as a way to address storage locations.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kavita Padmanabhan** whose telephone number is (571)272-8352. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Apu Mofiz can be reached on 571-272-4080. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kavita Padmanabhan
Patent Examiner
AU 2161

March 30, 2008

/Kavita Padmanabhan/